Austin Journal of Nanomedicine & Nanotechnology

Austin Publishing Group

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Editorial

Graphene Based Nano Electromechanical Interconnects to Enable Ultrafast Electronics

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Received: August 30, 2014; Accepted: September 08, 2014; Published: September 10, 2014

Editorial

Integration of nano electromechanical systems (NEMS) to current complementary metal oxide semiconductor (CMOS) chips significantly reduces the contact resistance of electronic devices and enables high speed electronics. However, NEMS devices suffer from packaging problems and their performance parameters in durability and reliability are low. Utilizing graphene in NEMS provides exceptional structural, mechanical, thermal and electrical properties for the interconnections and thereby constitutes a promising solution for high performance packaging and electronic applications.

Graphene is a collection of sp^2 bonded carbon atoms arranged in a two-dimensional honeycomb shaped lattice. It is optically transparent with highly accessible surface area and has an exceptionally high electrical conductivity. Its unique electrical properties such as ballistic electron transport are attributed to its planar conjugate bonds. Theoretically, graphene has the highest electron mobility (200000 cm^2/Vs), highest thermal conductivity (4000 W/mK), largest elastic modulus (10TPa), highest hardness (217 kgf/mm), largest yielding strength (6.4TPa) and largest tensile strength (130GPa that is three orders of magnitude larger than A36 steel's) among all known materials. We anticipate that hybridization of graphene with compatible materials (MoS_2, BN, and WS2) is going to create unique opportunities at nano scale. Optimization of such graphene based interconnections for specific devices such as sensors and transparent electrodes is very interesting for the N/MEMS community. The proposed interconnections are micro-bonded and encapsulated with light weighted and cost effective polymers providing high thermal resistance [1-8].

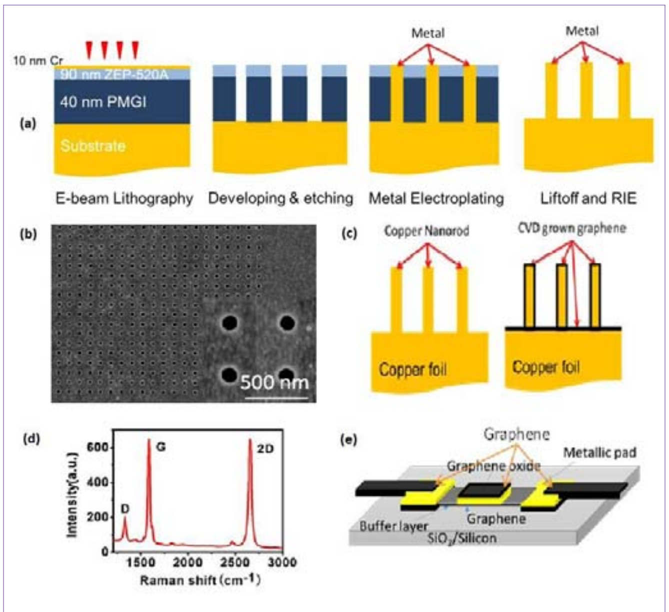

Figure1: (a) Schematic that demonstrates the fabrication steps. (b) SEM graph of fabricated nanowires. (c) Schematic diagram of graphene film deposition around copper nanorods/nanowires (d) Raman spectrum data of multilayer graphene films (e) Schematic diagram of graphene/metal nanostructure fabrication through lithography method and metal deposition as connection pad.

The fabrication of copper nano wire arrays, growth of graphene on the top of copper nano wire arrays, transfer of graphene coated nano wire arrays to graphene coated Silicon on SiO2 substrate, fabrication of contact pads and polymer encapsulation are the main steps of the device fabrication. These steps are briefly described in Figure 1. E-beam lithography and electroplating are followed by atomic force microscopy, scanning tunneling microscopy, four probe lock measurements at cryogenic temperatures for the copper nano wire array fabrication and characterization. Chemical vapor deposition of carbon forms monolayer graphene on nano wire arrays on which polymethyl methacrylate is spin coated and bulky parts of the copper foils are etched away by using an aqueous solution of $Fe(NO_3)_3$. Films are physically transferred to commercially available graphene coated SiO_2 on Si substrates on which metal electrodes are formed with ultraviolet lithography. The PMMA is then dissolved and removed by using conventional solutions. A few step special process recipes finalizes contact electrode and top gate fabrication as sketched in Figure 1 (e). Mechanical and electrical properties of the graphene integrated parts are tested by multiple techniques including AFM, SEM, transmission electron microscope (TEM), Raman Spectroscopy (RS) with various wavelength laser sources, nano-indentation and four-probe lock-in technique at cryogenic temperatures. At the graphene interfaces utilization MoS_2, BN or WS_2 buffer layers is of significant importance to achieve the desired performance parameters [9-12].

Interconnections are one of the most significant components of every electronic device. Recently, miniaturization of electronic devices required extensive utilization nanotechnology. In the present paper, we have proposed and demonstrated an interconnect that utilizes graphene hybridized NEMS. It provides durable and reliable packaging properties and is suitable for high speed electronics applications.

Citation: Yavuz M, Irannejad M, Alici K, Rahman EA, Brzezinski A and Cui B. Graphene Based Nano Electromechanical Interconnects to Enable Ultrafast Electronics. Austin J Nanomed Nanotechnol. 2014;2(6): 1033.

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Austin J Nanomed Nanotechnol - Volume 2 Issue 6 - 2014
ISSN : 2381-8956 | www.austinpublishinggroup.com

Citation: Yavuz M, Irannejad M, Alici K, Rahman EA, Brzezinski A and Cui B. Graphene Based Nano Electromechanical Interconnects to Enable Ultrafast Electronics. Austin J Nanomed Nanotechnol. 2014;2(6): 1033.