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Review on Single Electron Transistor (SET): Emerging Device in Nanotechnology

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Abstract

The main aim of this paper is to present a brief technical review on the physics of emerging nano-electronic device: Single Electron Transistor (SET). The manuscript deals with introductory overview of evolution in the field of nano-electronic devices as well as highlights the prospects of SET as an upcoming nanodevice to replace the conventional ones. SET operates on the principle of controllable transfer of single electron charge in between nano conducting islands. The remarkable device characteristics predominated by quantum mechanical characteristics of matter and shows novel traits of coulomb oscillation, coulomb blockade and quantum tunneling which is a boon for various applications. Because of its nanometer dimensions, SET offers ultra-low power dissipation and faster frequency of operation. SET; an innovative type of switching device that exhibits controlled electron tunneling to amplify current has although revolutionized the semiconductor industry but shows limitations like low voltage gain, accumulation of background charges and relatively large output resistance. To remove these restrictions it can be used along with Field Electron Transistor (FET). In this review paper there is a detailed description of SET, comparison of its different fabrication techniques along with future applications.

Keywords: SET; Tunneling; Coulomb blockade; Fabrication; FET; Applications

Introduction

Over the past five decades, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has emerged as basics of all computing devices and memory cells [1]. The main reason behind this popularity is continuous scaling of feature dimensions, which has recently entered the deep sub-micron range. Furthermore reduction in feature size is restricted by laws governed by quantum physics and hurdles imposed by fabrication systems. These restrictions pushes the researchers to explore new alternatives to conventional transistors for ultra-dense circuitry. These new devices having dimensions on the order of tens of nanometers are called *nano-devices* and their science is termed *nano-technology* [2]. The devices are classified into three broad categories based on the operating principles and fabrication techniques; 1) Carbon nanotube transistors, 2) Solid state quantum effect devices and 3) Molecular electronic devices. Devices in the first category are similar to the conventional MOSFET but are dissimilar in dimensions and in the material, as they are made of carbon nanotube. The second and third classes both use quantum effects but are fabricated differently. The solid-state devices use fabrication techniques similar to, those employed for MOSFETs. Molecular electronics is an innovative tactic, which requires new raw materials and a new operating principle.

Solid State Quantum Effect Devices exploits the benefits of quantum effects. An essential common feature of all these devices is a small island confining the conductive charge in the form of electrons. This island is analogous to the channel of a MOSFET. These devices based on electron confinement are bifurcated into two categories: Single electron and Quantum dots. The composition and device dimensions of islands gives the device its distinctive properties. Strategically controlling these parameters allows the device designer to flexibly employ quantum effects in a variety of styles to manage passage of electrons on to and off to the islands. This review paper deals with the first one, Single Electron Transistor (SET) in details.

The SET is a unique type of switching device that follows the phenomenon of regulated electron tunneling in order to amplify the current. A nano device can transfers a single electron at a time. The transfer of electrons is governed by Coulomb interaction and occurs on a minute conductive layer termed as island. SETs are considered to be the elements of the future. SETs will be used to produce highly dense and low powered integrated circuits, which will be able to detect the motion of individual electrons. During the discovery of single electronic tunneling and coulomb blockade mechanism , many researchers predicted that on shrinking the dimensions of quantum dots to nanometer range it is quite possible to manufacture applicable SETs [1,3].

SET is a three-terminal Single Electron Device (SED) which offers low power consumption and high Operating speed. In addition, as the size reaches to nano, quantum mechanical effects are came into action, which makes SETs to work more efficiently [4].

Contrary to conventional FETs which operates on principle that switching of transistor occurs when electron is appended or extracted from a semiconductor, SET can be made to turn ON or OFF each time a single electron is inserted into it. For the practical applications, it is necessary for the SET to be operated at room temperature. For

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this purpose, the size of the island of SET must be as small as possible [1,3,5-7].

History

Initially in 1968 phenomenon of electronic charge quantization was noted in metallic particle containing tunnel junction. Later on the concept that Coulomb blockade is over comes by gate electrode was suggested by number of researchers. Kulik and Shekhter developed the theory of Coulomb-blockade oscillations (the periodic variation of conductance as a function of gate voltage). Their theory was classical, including charge quantization but not energy quantization. The idea of SET was first proposed by Dmitri Averin and Konstantin Likharev in 1985. In 1987, Theodore Fulton and Gerald Dolan at Bell Labs in the US, created first SET (entirely out of metals) and observed the predicted oscillations. They made a metal particle connected to two metal leads by tunnel junctions, all on top of an insulator with a gate electrode underneath. Since then, the capacitances of such metal SETs have been reduced to produce very precise charge quantization .The first semiconductor SET was fabricated accidentally in 1989 by Scott-Thomasetal [1,3,5,8,7].

Schematic Circuit of Set

Similar to conventional FET the SET is also a three terminal device having a metallic island situated in between the 2 tunneling junctions; which joined to drain, source and gate electrode (Figure 1). These junctions are primarily fine oxide layers (<10nm) or thin insulating barriers between the island and the two conducting electrodes. Quantum dots have also been used as islands for the SET [10].

A small conducting island [Quantum Dot] coupled to source and drain leads by tunnel junctions and capacitively coupled to one or more gate, which is used to control the transfer of single electron from source to drain [11].

The conducting island is placed in between 2-tunnel junction having stored charge capacitance values as Cd and Cs. SET can electrostatically be steered by the gate capacitance CG. Hence, total effective capacitance of island is expressed as

$$C_{\Sigma} = C_D + C_S + C_G$$

Thus, such a set up is called single electron transistor [4]. Because of its unique structure, SET has many prospective characteristics such as low power consumption, high sensitivity, high switching speed, high packet density, etc. So much attention has been attracted on their fabrication and industrial realization [1].

Function of Coulomb Island (quantum dot)

Quantum dot (QD) having dia of the order smaller than 100nm is a type of mesoscopic system [12] (Figure 2). Here the alteration in electrostatic energy or coulomb energy is obtained by either removing or adding an electron with energy greater than heat energy and monitors the electron transport into and out of quantum dot. In other words, Quantum dot is a small conducting island that contains a tunable number of electrons occupying discrete orbitals [4,13,14].

Single-electron transistors have been made with critical dimensions of just a few nanometers using, Metals, Semiconductors, Carbon nanotubes, and individual molecules [3,11].

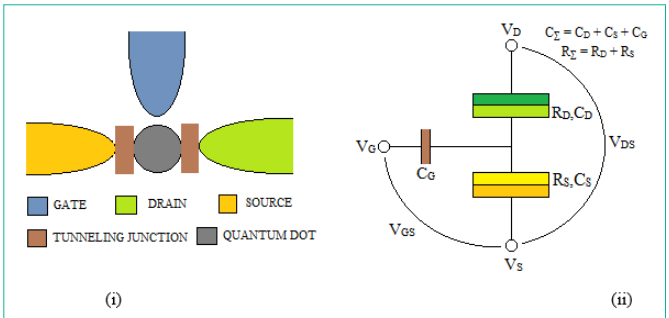

Figure 1: (i) Schematic Structure of SET; (ii) Equivalent Circuit of SET [9].

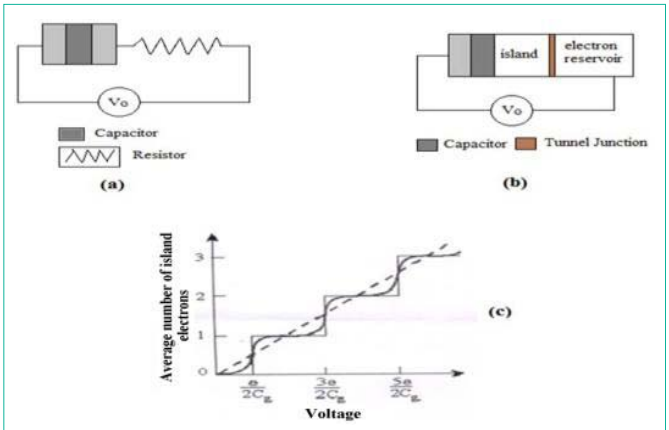

Figure 2: (a) When a capacitor is charged through a resistor, the charge on the capacitor is proportional to the applied voltage and shows no sign of quantization; (b) When a tunnel junction replaces the resistor, a conducting island is formed between the junction and the capacitor plate. In this case the average charge on the island increases in steps as the voltage is increased; (c) The steps are sharper for more resistive barriers and at lower temperatures [1].

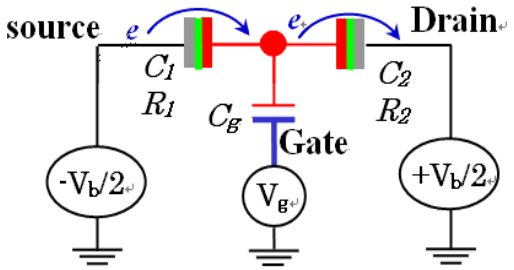

Figure 3: Working mechanism [22].

Working of Set

The SET monitors the electronic charge flow between drain and source with the assistance of gate electrode. The electrical behaviour of the device(if it easily let or not let the current to flow between source and drain) is a function of transport of single elementary charges and the voltage on gate node. When the Coulomb blockade is overcome, one electron will tunnel from the source to the island, adding one extra excess electron. Similarly, a tunneling process will occur from the island to the drain (Figure 3).

As SET offers a charge sensitivity of order of $10^{-6}e/(Hz)^{1/2}$; hence it can be made to operate as sensitive, linear charge amplifier by

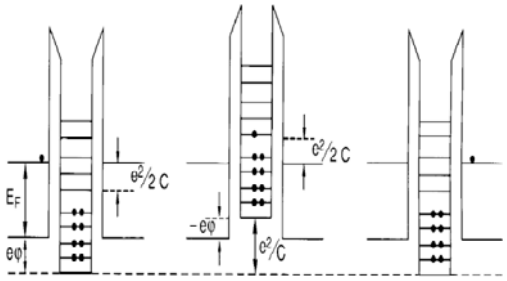

Figure 4: Energy level representation and moving of an electron from source to island and island to drain [15].

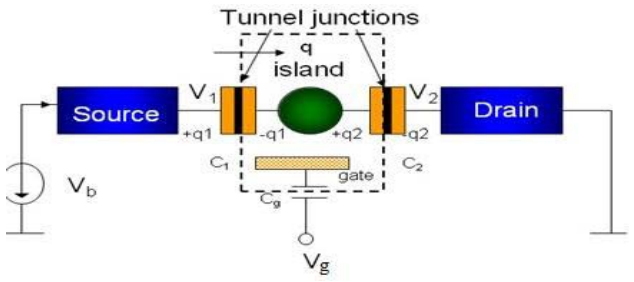

Figure 5: Schematic Diagram [20].

simply exploiting the single electron quantum tunneling effect. This represents that a charge variation of 10-6 e can be detected in a measurement time of 1 second [4] (Figure 4).

The principle of operation of SET devices can be explained based on laws of quantum mechanics; here energy levels are quantized and possesses natural number electrons as size reaches zero. Each band level possesses its distinct amount of energy, and to plunge from a certain band level to yet another band level possessing distinct energy, the electron either loses or gains energy depending whether moving from higher to lower or lower to higher energy level. It has been presented that this movement of electron is tunneling process of electron through tunnel junction [15-18].

The two main processes that take place in this nano structured electronic device are Coulomb blockade and single electron tunneling [19].

Main phenomenon required set to work

Coulomb blockade: Coulomb blockade can be defined by three factors:

- Coulomb energy.
- Tunnel resistance.
- Excess electrons.

Coulomb energy: A typical tunnel junction is actually a fine insulating strip acting as a barrier between the electrodes (Figure 5), which are conductive in nature. In accordance to principle of electrodynamics, insulating barriers restricts the flow of charge thereby preventing the current flow due to tunnel of electron from source electrode to island; there will be increase of the electrostatic energy of island which is given by,

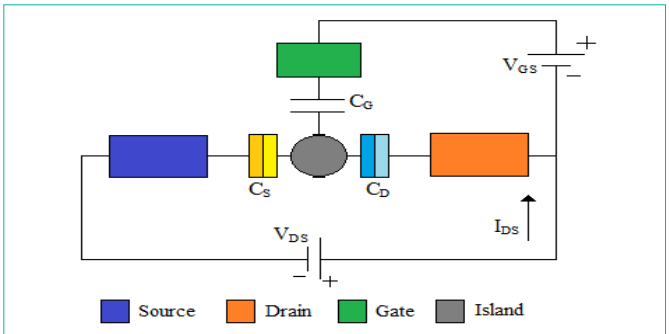

Figure 6: Circuit diagram of single island double tunnel junction SET [9].

$$E_c = e^2 / 2C$$

where C is the effective capacitance of the island.

Electrostatic energy denoted by Ec is also termed as coulomb blockade energy. This coulombing charge energy is amount of energy required to repel the upcoming electron by previous electron present within the island. In case of a tiny system, the capacitance C of the island is very small.

Thus, according to equation above, EC will be very high and due to this reason, electrons are unable to move simultaneously, but pass one-by-one. This phenomenon is known as "**Coulomb blockade**".

The suppression of electron transfer can be removed by one of these two possible cases:

(a) When the coulomb charging energy is overcome by thermal excitations at a temperature T, i.e

$$T \sim To = E_c / K_B$$

(b) When the coulomb charging energy is overcome by an externally applied voltage V, i.e.

$$V \sim V_t = E_c / e = e / 2C$$

where, Vt is known as "Threshold voltage" which is defined as an applied voltage that is just sufficient to increase the energy of electron above the coulomb blockade of tunneling so that the current can start to flow through the tunnel junction [4,5,13,21-26].

Tunnel resistance: Since, the tunnel junction is composed of two conductors and an insulating layer in between island and source electrode or drain electrode (Figure 6). Therefore, tunnel junction is described by the tunnel resistance R and tunnel capacitance C. In this case, tunnel junction acts as a capacitor and the insulating layer works as a dielectric medium for tunnel capacitor C.

As electron tunnels the junction, tunnel capacitance is charged with an elementary charge building up a voltage [V = e/C]. If the capacitance of the tunnel junction is very small, the voltage developed in the tunnel junction may be sufficient to prevent another electron to tunnel. In this situation, the electric current is suppressed if the bias voltage (V_{bias}) is lower than the Voltage (V) developed in the tunnel junction. Thus, the increment of the tunnel junction resistance around zero bias is considered as the coulomb blockade.

Therefore, coulomb blockade may be defined as the increased tunnel junction resistance at very low bias voltages of an electronic

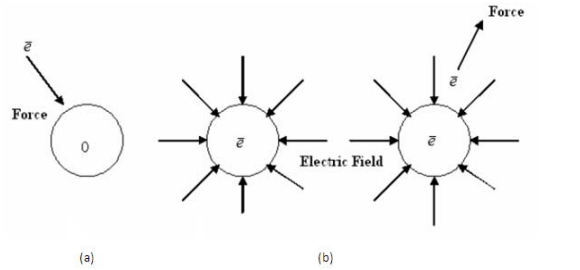

Figure 7: a) an electron feeling a small attractive force as it approaches a sphere; b) Once sphere gets charge by a single electron; other electrons will feel a strong repelling force [4].

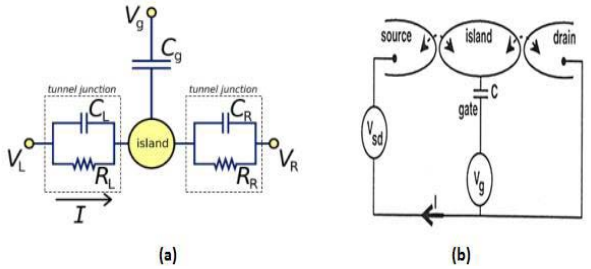

Figure 8: (a) Circuit diagram of SET with current flow; (b) schematic circuit with current flow.

device, which consists of at least one low capacitance tunnel junction.

The coulomb blockade can be achieved only if, in case, when the following three conditions meet:

1. The bias voltage must be lower than the elementary charge divided by the self-capacitance of the island. i.e,

$V_{bias} < e/C$

2. The thermal energy KBT must be below the charging energy i.e.,

$K_{BT} < e^2/C$

or else the electron will be able to pass the quantum dot (QD) via thermal excitation.

3. The tunneling resistance (R_T) should be greater than $h/2\pi e^2$, which is derived from "Heisenberg's uncertainty principle". i.e,

$R_T > h/2\pi e^2 = 25813\Omega$

This is the required condition for tunnel resistance [4,5,21-28].

Excess electrons: a) an electron feeling a small attractive force as it approaches a sphere. b) Once sphere gets charge by a single electron; other electrons will feel a strong repelling force [4] (Figure 7).

The island contains a very large number of electrons ($\cong 10^9$). Through tunneling, there is an addition or subtraction of electrons from the island charging it either negatively or positively. The extra electrons that charge the island are called excess electrons and their number is designed by *n*.

The presence of excess electrons affects the electrostatic energy of the system, which depends on the charging energy of the SET:

$$E_{th} = \frac{1}{2}\frac{Q_{isl}^2}{C_\Sigma} = \frac{1}{2}\frac{n^2e^2}{C_\Sigma}$$

where Q_{isl} is the charge on the island, n the number of excess electrons, e the charge of one electron and C_Σ the total capacitance of the island which is equal to:

$C_\Sigma = C_G + C_S + C_D$

The energy does not only depends on Q_{isl}, but also on the charge induced by the gate, the gate charge

$Q_G = V_G C_G$

where V_G is the gate voltage.

The electrostatic energy of the system is equal to

$E_{el} = E_c(n\text{-}n_g)^2$

where *n* is the number of excess electrons of the island and

n_g the number of elementary gate charges.

The expression for the electrostatic energy of the system then becomes:

$$E_{el} = \frac{1}{2}\frac{Q^2}{C_\Sigma} = \frac{1}{2}\frac{(ne - V_G C_G)2}{C_\Sigma} = \frac{1}{2}\frac{(ne - Q_G)^2}{C_\Sigma}$$

This energy determines if tunneling through a junction is forbidden or allowed: if the adding of an extra excess electron causes the energy of the system to increase then tunneling will be energetically forbidden and the Coulomb charging energy will act as a blockade. This is known as the Coulomb blockade [29].

Based on the Coulomb blockade effects, many interesting devices are possible such as precise current standards, very sensitive electrometers, logic gates and memories with ultra-low power consumption, down scalability to atomic dimensions, and high speed operation.

Tunneling of Single Electron: When the Coulomb blockade is overcome one electron will tunnel from the source to the island, adding one extra excess electron. Similarly, a tunneling process will occur from the island to the drain.

For functioning of SET or for tunneling process :

- Capacitance of the island must be less than 10^{-17} Farads and therefore its size must be smaller than 10nm.
- The wavelength of the electrons is comparable with the size of the dot, which means that their confinement energy makes a significant contribution to the coulomb energy (Figure 8).

Fabrication of Set

According to the main procedures, the fabrication methods are of two types- Physical method and chemical method.

Physical method

The physical methods often utilize the combination of thin film and lithographic technologies. Devices with carefully tailored geometries and electron density are got.

Chemical method

Recently many wet chemical techniques are used for the synthesis

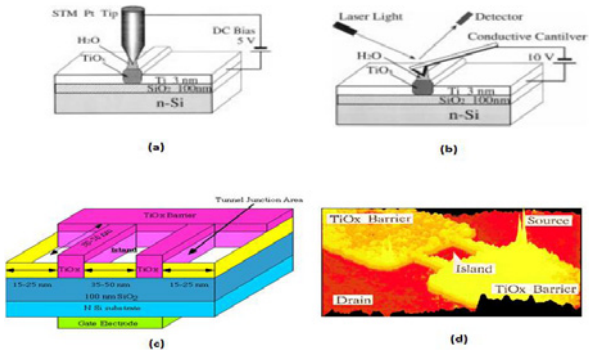

Figure 9: (a) The principle of STM nano-oxidation process. Tip of STM was made of platinum 100nm SiO_2 was thermally formed. Titanium was deposited by Evaporation [36]; (b) Principle of AFM nano-oxidation process. Cantilever of AFM was made conductive by evaporating Au metal or Ti metal [36]; (c) Picture of an titanium SET [3,37]; (d) Picture of SET using an ATM [3].

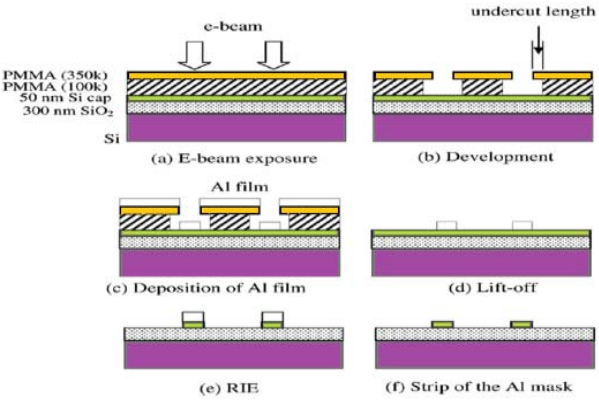

Figure 10: The schematic diagram showing the process flow for the fabrication of SOI SET's [34].

of various nanostructures [30-32]. This approach is prosperous for its low cost and good controllability of the size of Coulomb islands, and it is possible to be a prospective technique. Though this technique is not mature industrially [1].

Different fabrication techniques of set: There are many techniques used for fabrication of SET such as Electron Beam Lithography, STM/AFM, Fabrication of SET using Carbon Nano Tube (CNT) using E beam irradiation etc.

STM/AFM nano oxidation process

SET is using a Scanning Tunneling Microscope (STM) and can avoid the control problems in self- organized structures. Using this technique an SET can be created that operates at room temperature.

The Process: A 3nm Titanium (Ti) metal film is deposited on a 100nm thermally oxidized SiO_2/n-Si substrate. The Ti surface is oxidized by through the water on the surface via the atmosphere. By using the STM tip as a cathode nanometer size Ti oxide (TiO_x) lines can be formed. The barrier height of a TiO_x/Ti junction has been found to be 285 meV for the electron from the temperature dependence of the current [33-35] (Figure 9).

Electron beam lithography

Figure 10 demonstrates the process flow for the fabrication of

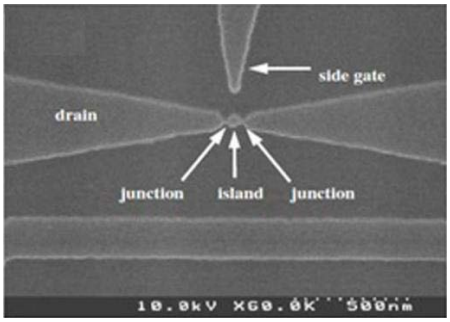

Figure 11: The Scanning Electron Microscope Image (SEM) of fabricated SET device on SOI using Electron Beam Lithography.

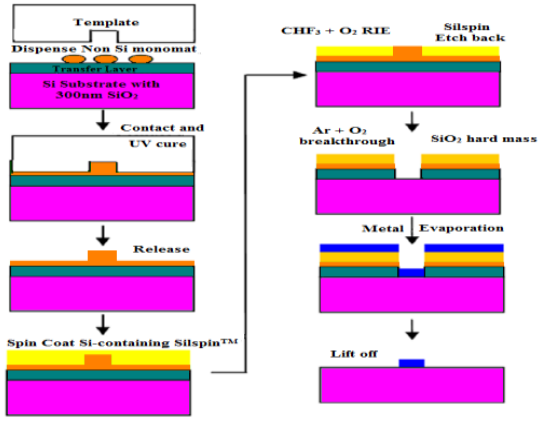

Figure 12: Detailed SFIL-R imprint process flow.

SOI SET devices. The SOI substrate used has an n-type 50nm thick Si capping layer on a (100) Si surface, sandwiched by a 300nm thick buried oxide layer. The carrier density of the Si capping layer is 2.1019cm^3 and the resistance is 3.102Xcm. A bilayer of PMMA resists (the molecular weight of 100k on the bottom and 350k on the top) was first spin coated on the SOI substrate and baked at 180°C for one hour in oven. A high-resolution electron beam lithography system, VB6 HR from Leica Cambridge was used to write the SET patterns at the electron beam acceleration voltage of 100kV and the beam current of 500pA. Development was carried by a standard MIBK:IPA (1:3) developer at room temperature followed by rinse in IPA for 30 seconds and finally blow dry by a compressed air. The etching using in figure 10 (e) is reactive ion etching using Fluorine based plasma. Metallization was done with Cr and Al and it was found that Al shows much higher lift off than Cr [34] (Figure 11).

Step and Flash Imprint Lithography (SFIL)

SFIL is low temperature, low pressure, Ultra Violet based Nanoimprint Lithography (UV-NIL). It is advantageous because it can avoid complicated changes in process parameters for multi layer imprints due to large changes in temperature and pressure. The other main advantage is that this technique can be used for mass production [34] (Figure 12 &13).

Controlled fabrication of single electron transistors from single-walled carbon nanotubes

Metallic grains and colloidal nanocrystals give smaller sized

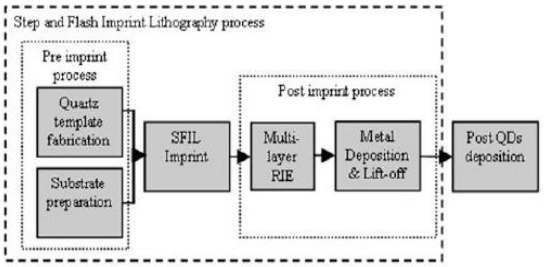

Figure 13: The flowchart for SET for mass production using SFIL.

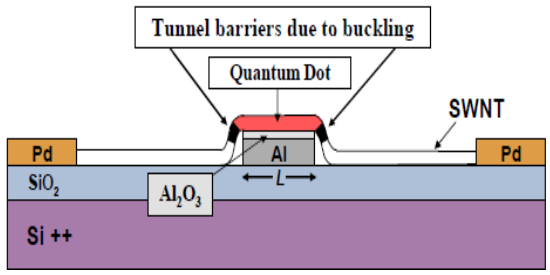

Figure 14: (Color online) (a) Schematic diagram of the nanotube SET device. The nanotube bends at the edges of the Al/Al_2O_3 gate electrode to create two tunnel barriers (black) a distance (L) apart. The central island (red) in between the tunnel barriers above the aluminum oxide is the defined quantum dot. The gate defines the quantum dot and controls its operation.

uniform dots with SET operating temperature ~100K, however, for SET operation they need to be placed in Nano sized gaps, which is highly challenging and difficult to control giving an extremely low device yield. Recently, nanowires and Single Walled Carbon Nanotubes (SWNTs) have been considered good candidates for the fabrication of SETs and as interconnect because of their small diameters [38].

Fabrication of SET using SWNT relies on the introduction of tunnel barriers. It has been shown that when a SWNT is bent at a selected position, the bend acts as a nanometer sized tunnel barrier.

By creating a pair of bends on an individual SWNT using AFM tip, SETs have been demonstrated. A cartoon of our device is shown in Figure 14. A SWNT is placed on a 100nm wide local Al/Al_2O_3 bottom gate and then contacted with Pd source and drain electrodes of 1μm separation on Si/SiO_2 substrates.

The aluminum gate serves three purposes: (i) it acts as a "mechanical template" to define two tunnel barriers at the edges by naturally bending the nanotube due to van der Walls interactions with the substrate17, (ii) the width of the gate defines the size (L) of the quantum dot, and (iii) it acts as a local bottom gate to control the operation of the SET device. Low temperature electronic transport measurements show Coulomb oscillations up to 125K. The stability diagram shows charging energies of 12-15 meV and energy level spacing of ~5meV. These energies are in agreement with a quantum dot size of ~100 nm, thus verifying the dot is defined and controlled by the local gate.

The device is fabricated on heavily doped Si wafers with a 250 nm SiO_2 capped layer. Larger features such as contact pads are first defined by photolithography using double layer resist (LOR 3A/ Shipley 1813), developed in CD26, followed by thermal evaporation of 5nm thick Cr and 40nm Au, and standard lift-off. We then define arrays of 40μm long and 100nm wide patters by means of Electron Beam Lithography (EBL) for the Al gates along with reference markers (to later connect the NTs), followed by 40nm of thermal Al deposition and lift-off in acetone. A thin aluminum oxide layer is created by oxygen plasma treatment for 10 minutes to serve as a gate dielectric. CVD grown SWNTs (cheaptubes.com) are then ultrasonically dispersed in 1,2- dichloroethane (DCE) for ~5 minutes. The average length of the nanotubes after dispersion is 2-5 μm, determined by AFM. The nanotubes are then spun (~1000rpm) on the substrate containing the array of Al gates. By tapping mode Atomic Force Microscopy (AFM), we locate the nanotubes that pass over the Al/Al_2O_3 gate and record their coordinates with respect to the reference markers. Another step of EBL is then implemented to define Source (S) and Drain (D) top contacts, followed by 25nm of Pd deposition and lift-off. Pd was used to make good contact with SWNT to avoid additional tunnel barrier formation at the nanotube source-drain interface.18 Devices are bonded and loaded into a 4K cryostat for electronic transport measurements. Nine devices were measured all with 100nm local gate [39].

Fabrication technique for carbon nanotube single-electron transistors using focused ion beam

Figure 1 shows a schematic of a nanotube SET fabricated using a FIB (Seiko Instruments Inc. SMI9200). The acceleration voltage and minimum diameter of the Ga^+ ion beam were 30kV and 7nm, respectively. $W(CO)_6$ gas was used for the ion-beam-assisted deposition of tungsten (W) for the nanoscale wiring to the CNT. The substrate was a heavily doped p^+-silicon wafer with a thermally grown oxide (100nm). The fabrication process was as follows. First, contact pads of Ti/Au (100/200 nm) were formed on the wafer by photolithography, metal deposition, and the lift-off process. The bottom metal surface was used as a gate electrode. Second, MWNTs synthesized by arc discharge were dispersed on the wafer. The positions of the MWNTs were measured by the Scanning Electron Microscopy (SEM).

Then, W nanowires from each end of the MWNT to the contact pads were deposited by using FIB-assisted deposition. Finally, two trenches were formed on the MWNT by FIB etching. The W deposition was performed under the following conditions; the diameter, the current, and the dose of the Ga^+ ion beam were 18nm, 3.6pA, and 1.3x1018 cm^{-2}, respectively. The fabricated W wire was 80nm wide and 30nm thick. The resistance of the W nanowire was proportional to its length, and the resistivity was $2.2x10^{-4}$Ωιcm. Although this resistivity is much higher than that of bulk tungsten ($5x10^{-6}$Ωιcm), the resistance of the W nanowire is sufficiently small for use as an electrode of nanotube devices [40,41] (Figure 15).

Single electron transistor fabrication using focused ion beam direct write technique

Single Electron Transistors are fabricated in a series of process steps utilizing high beam currents and low beam currents available on the FIB. Lower beam currents are used to fabricate nano scaled structures, which require smaller energy doses, whereas higher beam currents are used to realize the micro scaled structures. The process flow for the fabrication of SET by FIB direct write technique is shown

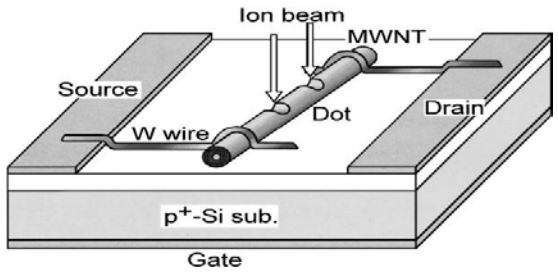

Figure 15: Schematic of nanotube SET fabricated by using FIB.

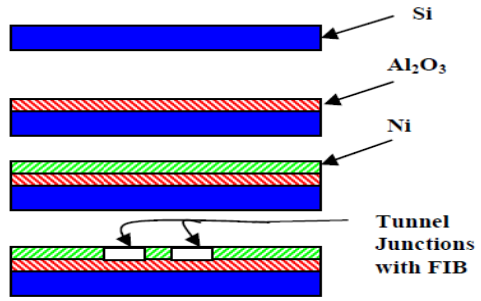

Figure 16: Process flow for SET fabrication on Si using FIB.

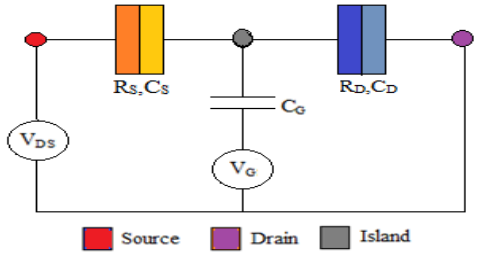

Figure 17: Single electron transistor circuits with Single Island.

in the Figure 16.

A 150nm thin film of Al_2O_3 is deposited on a clean silicon wafer using a Radio Frequency (RF) sputter deposition Perkin Elmer 2400-8J parallel plate-sputtering system. Following the deposition of Al_2O_3, a 50nm thin layer of Ni is deposited using the same system [42].

I-V Characteristics of Set

From the IV- characteristics of the SET for $|V| < e/C_\Sigma$, the current is zero. This state is called Coulomb blockade (Figure 17&18). Hence, if the bias is low, the tunneling of electron will not take place. Now, if the applied bias junction voltage Vbias is increased above the threshold voltage Vt by charging energy, the effect of Coulomb blockade can be removed and the current flows. In this condition, the junction behaves like a resistor. Figure 19 represent the IV-Characteristics for a highly asymmetric junction circuit for RS << RD.

In this case, there is a rapid movement of excess electrons from one junction to another which increases the total charge of the island. If the bias voltage is increased, the population of electrons in the island also increases. In this case the IV- Curve represents Stair-like characteristics, which are commonly referred to as the "**Coulomb Staircase**" [4].

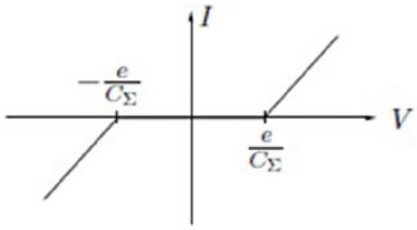

Figure 18: I-V characteristics of SET for symmetric junction.

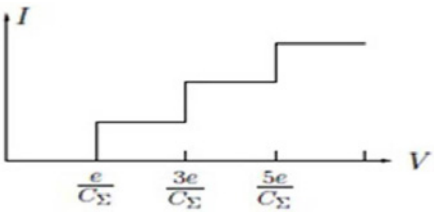

Figure 19: I-V Characteristics of the SET for asymmetric junction representing "coulomb Staircase state".

Advantages

- Compact size
- Low energy consumption
- High sensitivity
- High operating speed
- Simplified circuit
- Feature of reproducibility
- Simple principle of operation
- Straight forward co-integration with traditional CMOS circuits [4,21,43,44].

Disadvantages

- Integration of SETs in a large scale

To use SET at room temperature, the necessary condition is that the size of island must be less than 10nm which is very difficult to fabricate.

- Linking SETs with the outside environment
- Practical difficulty in fabrication
- Most SETs works at extremely low temperatures around 100mK
- Background charge problem
- Low voltage gain
- The voltage increases until the charging energy is of order k_bT, then it drops [4,10].

Problems

Gain

In SETs, voltage gain decreases as the size of device decrease

because of the low gate capacitance. It is difficult to achieve a large gate capacitance when the island of a SET consists of a single electron. For the single electron devices, the gate capacitance can be as small as a few zepto Farads. And for this the required bias voltage is tens of volts so that the output can be modulated by tens of millivolts which results in voltage gain of the order of 0.001 i.e., the transistor attenuates the signal by a factor of about 1000.

The voltage gain in SET is the ratio of the gate capacitance to the junction capacitance. As the gate, capacitance is increased for fixed junction capacitance and fixed temperature, the voltage gain first increases and then it decreases. The voltage gain increases with increasing gate capacitance until the charging energy is on the order of k_BT and then the voltage gain drops sharply.

However, in transistor voltage gain is not a very useful factor. For SETs, it is more relevant to consider the charge gain. The charge gain is the modulation of the charge that passes through the SET divided by the change in charge on the gate. This is a frequency dependent quantity. It is also become possible to transport more charge through the SET than was added to the gate. Charge gain can easily be achieved at room temperature. The charge gain is maximum at low bias voltages and low temperatures

$$g_{charge} = (dI/dV_{g1})/(2\pi fC_g) = 1/(2\pi fRC_\Sigma)$$

Here f is the frequency at which the charge is modulated and R is the lower of the two junction resistances [45,46,7].

High output impedance

SETs have large output impedance of the order of at least 100kΩ which makes it an intrinsically slow device. To speed up the charge measurement, conventional Field-Effect Transistors (FET's) should be placed as close as possible to the SET. The FET can then buffer the high output impedance of the SET. However, using both at same circuit is a difficult task [45,46,7].

Background charges

There is another problem with SETs, which is the background charge problem. This problem arises because of the high charge sensitivity of SETs. A single charged vacancy or an interstitial ion in the oxide near a SET can be enough to switch the transistor from the being conducting to being non-conducting. The only effective way to compensate for this problem is to use field-effect transistors to tune the background charges away [45-47], [7,21,48].

The three problems of low gain, high output impedance, and sensitivity to background can all be remedied by combining SET's with FET's.

In such hybrid circuits, the SET's provide the charge sensitivity while the FET's provide the gain and the low output impedance.

One of the process in order to combine these two is as follows: In order to design SET/FET circuits, it is important to have a simulation package that will model both SET's and FET's. The simulation package SPICE is one of the few packages that will do this. Figure 20(b) shows a single-electron transistor that is current biased by a FET and the corresponding SPICE simulation of the circuit. A second FET is used to buffer the output of the SET which increases the speed of the circuit [45,49,50].

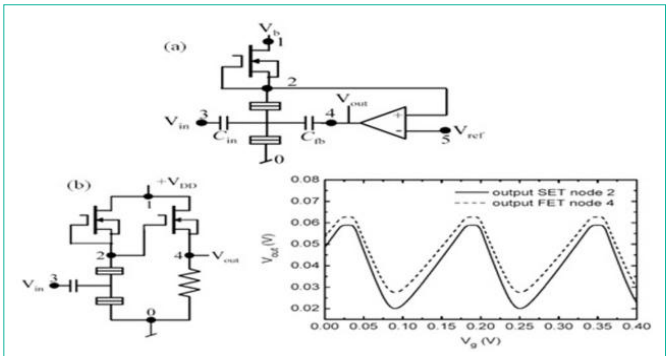

Figure 20: (a) A charged lock loop that automatically tunes away the background charge. Provided that the amplifier has enough gain, the voltage gain in this circuit is set by the ratio of the input and output capacitors Cin/Cout. The linearity and the dynamic range of the charge measurement are also improved by the charge-locked loop. The FET is used to current bias the SET. (b) The schematic of a current biased SET with a FET output stage and the corresponding SPICE simulation. The solid line is the voltage at the output voltage of the SET stage (node 2), and the dashed line is the voltage at the output of the FET stage (node 4). A voltage of 0.4 V has been subtracted from the voltage at node 4 to remove a dc offset.

Applications

Single electron memory

SET can be used as memory cell because of the state of Coulomb Island can be changed by the existence of one electron. In this way, SET enhances the capacity of memory devices that stores the information as the presence or absence of single electron on the island of SET. SETs also surpass the functionality of CMOS with such application. However, it is very difficult to fabricate such device. Although scientists are still working for it and if the fabrication becomes possible then it will be a revolutionized change in area of quantum computing [7,11,43,51-53].

High sensitivity electrometer

SET based electrometer is said to be operating by capacitively coupling external charge source to be computed to the gate node and then alteration of source-drain current is calculated. Due to enormous value of amplification coefficient, this device is used for calculating small change of current. Experiments showed that if there is a charge change of e/2 on the gate, the current through the Coulomb Island is 10^9e/sec. This sensitivity is many orders of magnitude better than common electrometers made by MOSFIT. SETs have already been used in metrological applications as well as a tool for imaging localized individual changes in semiconductors [7,11,23,43,47,48,54-58].

Microwave detection

If black body radiation is incident on SET, the photon-aided tunneling will affect the charge transfer of the system. Even a small amount of radiation will affect the SET system. The sensitivity of this equipment is about 100 times higher than the current best thermal radiation detector [7,11].

Single-electron spectroscopy

One of the most important application of single-electron electrometric is the possibility of measuring the electron addition energies (and hence the energy level distribution) in quantum dots

and other nanoscale objects [7,11,23,47].

DC current standards

Single-electron tunneling is fundamental standards of dc current for such a standard a phase lock SET oscillations or Bloch oscillations in a simple oscillator with an external RF source of a frequency f. The phase locking would provide the transfer of a certain number [m] of electrons per period of external RF signal and thus generate dc current which is fundamentally related to frequency as I=mef. This arrangement have limitation of coherent oscillation that can be overcome by the use of such a stable RF source to drive devices such as single-electron turnstiles and pumps, which do not exhibit coherent oscillations in the autonomous mode [7,11,47].

Temperature standards

One new avenue toward a new standard of absolute temperature can be developed by the use of 1D single-electron arrays. At low temperatures, arrays with N>>1 islands exhibit dc I-V curves generally similar to those of single-electron transistors with a clear Coulomb blockade of tunneling at low voltages ($|V|<V_t$). If the temperature is raised above E_c/kB, thermal fluctuations smear out the Coulomb blockade, and the I-V curve is almost linear at all voltages:

$$G \equiv dI/dV \approx G_n \equiv 1/NR$$

The only remaining artifact of the Coulomb blockade is a small dip in the differential conductance around V=0 [7,11,47].

Detection of infrared radiation

The Single electron array have the advantages of lower shot noise and convenient adjustment of the threshold voltage which would make it able to detect the few-tetra hertz frequency region, where no background-radiation-limited detectors are yet available [7,11, 43,47,59].

Voltage state logics

Voltage State Mode (VSM) can be applied to operate SET device. Here in VSM the applied potential VG on gate electrode steers the source to drain current. Thus, the single electron charging effects are within the transistor whereas externally it appears to be a usual electronic device, which switches multi electronic charge current, with binary logic 1 and 0 representing dc HI/low voltage levels. The demerit of VS circuits is that none of transistors in the complementary pair is near too well, so that the static leakage current in these circuits is present which is of the order of 10^{-4} e/RC. The corresponding static power consumption is negligible for the devices operating at helium temperatures and for the devices operated at room temperature, this power is of the order of 10^{-7} Watt per transistor. Hence there will be an unacceptable static power dissipation density (>10kW/cm^2) for the hypothetical circuits which would be dense enough (>1011 transistors per cm^2) to present a challenge for the prospective CMOS technology [7,11,25,47,60,61].

Charge state logics

Charge state logic is a device in which single bits of information are presented by the presence/absence of single electrons at conducting islands. In these circuits, there is no dc current in static state, hence, static currents and power vanishes. By using this device, the leakage current problem can be overcome [7,11,47].

Programmable single electron transistor logic

SET offering nonvolatile memory functionality can be applied for fabrication of programmable logic. During half of the period phase shift, the binary functional logic of SET is not or complementary of traditional SET. As a consequence of which SET can be operated as simple n-MOS SETs or complementary p-MOS SETs. By utilizing this fact, the function of SET circuit can be programmed based on function stored by the memory function. The charged around the QD (*viz.* island of SET) shifts the phase of coulomb oscillation. The writing/ erasing operation of memory function, which inject/eject charge to/ from the memory node near the SET Island, makes it possible to tune the phase of coulomb oscillation [7,11,21,43,62,63,64-71].

Conclusion

This review paper focuses on the general introduction, different fabrication techniques, and applications of SET. SET is a future device that makes the integration technology to reach the new level of technology. By using SET, electronic devices can be fabricated having low power consumption and high operating speed. However, SET is being applicable at low temperature. For making the SET to use in mass market, it must be operated in room temperature but due its limitations such as low voltage gain, high output impedance and background charges at room temperature, it cannot be more efficient. Hence, there are many techniques used by scientists to make SET in room temperature. Although all the techniques are still not be using for mass production of SET. In addition, for SET to use in its most efficient condition it is combining with FET to increase the voltage gain, decrease output impedance and surpasses background charges. Due to SETs one-to-one electron tunneling, it will be very useful in many applications especially in quantum computer and memory devices.

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